29C93A

ECMA 102/V110 Terminal Rate Adaptor Circuit (TRAC)

Description

The 29C93A is a Terminal Rate Adaptor Circuit (TRAC) performing speed adaptation between synchronous/asynchronous V24 terminals through ISDN 64 kbps “B” channel.

The TRAC can be connected to “B” channel using a programmable serial bus interface SLD, IOM... Programming is made in CLKSEL register.

The Master clock signal (7 or 12 MHz) is applied to input MCLK.

In asynchronous mode it is possible to exchange data between two terminals working at different speeds but using the same intermediate rate.

For synchronous terminals, the TRAC is able to work with network independent clocks, without addition of external circuits for phase compensation.

In X21 applications, the TRAC/V24 interface should be directly connected to the X21 controller 29C921 serial interface.

The Inband Parameters Exchange (IPE) is supported by the 29C93A. During initialization the microcontroller sends a set-up message through the TRAC µP interface. Parameters exchange is achieved through“B” channel on a byte basis at 64 kbps. Distant terminal parameters are sent through parallel port and processed by the external microprocessor, using external memory for buffering.

Synchronous IPE facilities provided are : On transmit side, IPE signals (State or Command) may be sent to distant TE many times (more than 32 times as specified in ECMA123) without µP bus load increase (auto-repeat transmission allowed in sync. IPE). On receive side, IPE signals FF (INACTIVE), FE (IDLE), FB (FILL), ... will be filtered so that they are detected during the first reception (interrupt generation) and ignored during the following receptions.

V25 bis protocol (call establishment) is also supported in async. mode by connecting the µP bus to the V24 interface.

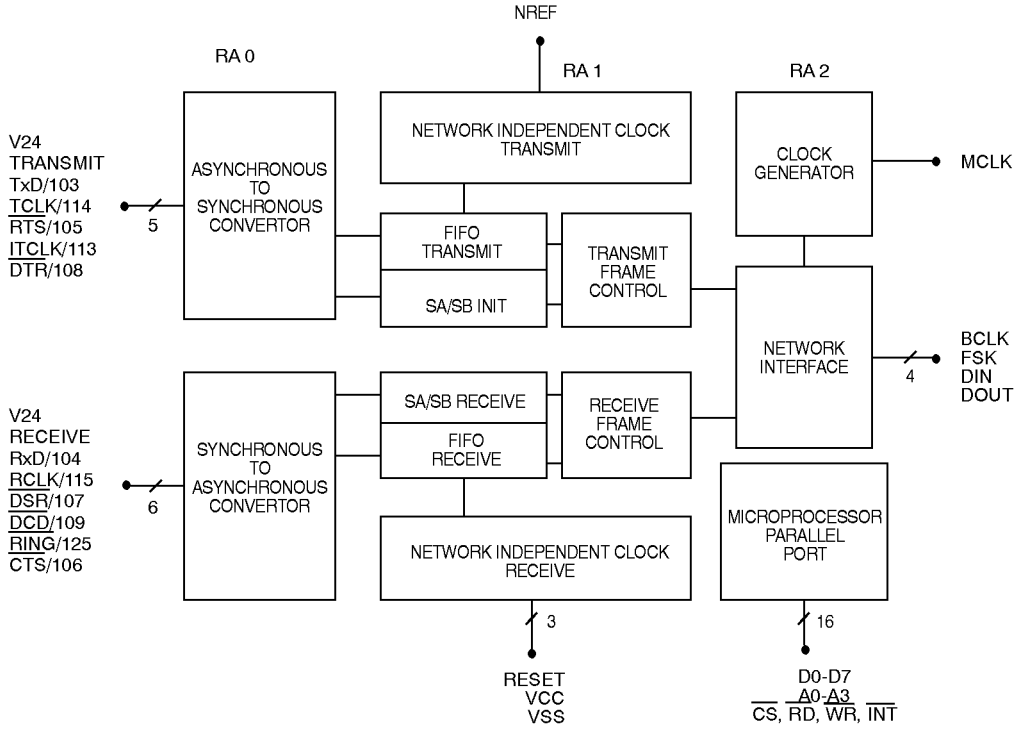
The TRAC together with ISDN layer 1/2 circuit using IOM/SLD/SSI interface provides a cost effective solution for implementation of a V24/ISDN Terminal Adaptor.

Features

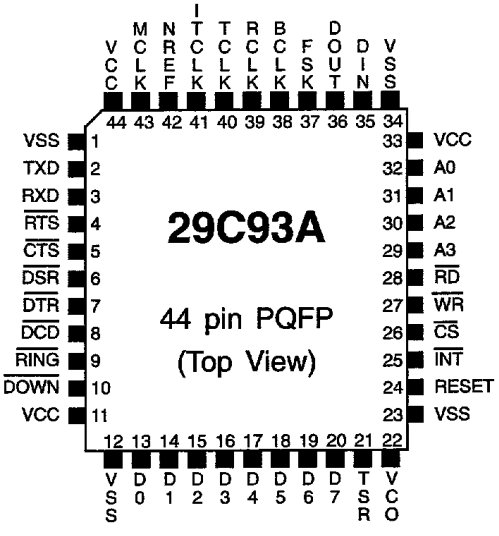
- Network independent clock supported in SYNC mode
- Rate adaptation between V24 terminal and ISDN B channel
- Full ECMA 102/V110 processing for SYNC. and ASYNC. terminals
- 50 to 57600 bps user data rates for asynchronous transmissions
- 600 to 64000 bps user data rates for synchronous transmissions
- IPE control characters processing (XSTART, FILL, OFF, IDLE...)
- “End to End” or “local” flow control capability using XON/XOFF or 105/106 circuits
- Easy interface with X21 terminals through X21 controller 29C921
- V25bis protocol compatible (call set-up through µP bus)
- In band parameter exchange (ECMA123 IPE) via µP bus
- Transparent mode capability (64 kbps)
- V24 interface
- 8 bit microprocessor interface
- Programmable serial system interface (IOM, SLD, SSI ...)
- Programmable escape character
- Power down mode
- Package = PQFP 44

Interface

Block Diagram



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	IN/OUT
13-20	D0:D7	BIDIRECTIONAL DATA BUS	IN/OUT
29-32	A0:A3	REGISTER ADDRESS BUS	IN
26	$\overline{CS}$	CHIP SELECT (ACTIVE LOW)	IN
28	$\overline{RD}$	READ SIGNAL (ACTIVE LOW)	IN
27	$\overline{WR}$	WRITE SIGNAL (ACTIVE LOW)	IN
25	$\overline{INT}$	INTERRUPT SIGNAL (ACTIVE LOW)	OUT
38	BCLK	SYSTEM BUS BIT CLOCK	IN*
43	MCLK	BAUD RATE MASTER CLOCK (12/7 MHz)	IN*
42	NREF	NETWORK REF CLOCK (192/512/1536/2048 kHz)	IN*
35	DIN	SYSTEM BUS DATA INPUT	IN*
36	DOUT	SYSTEM BUS DATA OUTPUT	IN/OUT
37	FSK	SYSTEM BUS FRAME SYNC (8 kHz)	IN*
41	ITCLK	V24 (113) CIRCUIT (NETWORK INDEP. CLOCK)	IN*
40	TCLK	V24 (114) CIRCUIT	OUT
39	RCLK	V24 (115) CIRCUIT	OUT
2	TxD	V24 (103) CIRCUIT (DATA TRANSMISSION)/X21 (T)	IN*
3	RxD	V24 (104) CIRCUIT (DATA RECEPTION)/X21 (R)	OUT
4	$\overline{RTS}$	V24 (105) CIRCUIT (REQUEST TO SEND)	IN*
5	$\overline{CTS}$	V24 (106) CIRCUIT (CLEAR TO SEND)	OUT
6	$\overline{DSR}$	V24 (107) CIRCUIT (DATA SET READY)/X21 (I)	OUT
7	$\overline{DTR}$	V24 (108) CIRCUIT (TERMINAL READY)/X21 (C)	IN*
8	$\overline{DCD}$	V24 (109) CIRCUIT (DATA CARRIER DETECT)	OUT
9	$\overline{RING}$	V24 (125) CIRCUIT (CALL INDICATE)	OUT
10	$\overline{PDWN}$	POWER DOWN	IN*
24	RESET	RESET INPUT	IN*
21	TRS	TRANSMISSION START	OUT
1-12-23-34	VSS	GROUND	
11-22-33-44	VCC	POSITIVE SUPPLY (+ 5 V)	

* with internal pull-up resistor.

Functional Description

Asynchronous Mode

Data Format

The TRAC can be programmed (in FASYNC register) to receive following data formats (parity included) :

5 bits with parity
5 bits without parity
6 bits with parity*
7 bits with parity
7 bits without parity
8 bits without parity
8 bits with parity
9 bits with parity*

The parity can be odd, even, forced low, forced high. The number of stop bits can be 1,1.5,2 (see table 2 in &5.1.1. of ECMA 102 rec.) except for (*) which have a number of stop bits automatically fixed to 1 (if parity is used). Concerning the parity bit, and when the buffers are used (RLBUFF, RDBUFF, TLBUFF or TDBUFF), the TRAC behaves as follows :

In reception : the parity test (if parity is used, that means [P0, P1, P2] not equal to [0, 0, 0]) is reported in INT0 register (PARL bit on local side, PARD bit on distant side).

In transmission : The parity bit is calculated by the TRAC for all data formats. This parity bit can be forced right (by writing in TLBUFF or TDBUFF) or forced wrong (by writing in ERRTL or ERRTD). This feature is specially useful in flow control mode using 9 bit data format. For example, if data is received with an erroneous parity bit, it can be sent with the same erroneous parity bit using a single write in ERRTL (on local side) or in ERRTD (on distant side).

Break Management

The TRAC will also handle BREAK signal as specified in ECMA 102/V110 recommendation. If the circuit detects M to 2M + 3 bits of start polarity where M is the number of bits per character in the selected format including start/stop bits, it will transmit 2M + 3 bits of start polarity. If the circuit detects more than 2M + 3 bits of start polarity, it will transmit all these bits of start polarity. The 2M + 3 or more bits of start polarity, received from the transmitting side of a remote terminal shall be output to the receiving local terminal. The TRAC must receive from terminal/modem at least 2M bits of stop polarity on circuit 103, before being able to send further data characters (terminal or modem resynchronization).

Speed Adaptation

The overspeed and underspeed control will be automatically performed by the TRAC (&5.2.2. of ECMA 102/V110 rec.). If frames with only one stop bit per character are assembled, only one stop bit every 8 character might be removed by transmit controller. When overspeed is detected, the receiver will re-insert the deleted stop bit.

The TRAC circuit supports all ECMA 102/V110 specified asynchronous speeds (see table 1 below). Different speeds can be programmed in the receive and transmit path. Consequently terminals with different speeds can be connected. According to ECMA 102 specification, the 2 terminals must use the same intermediate rate.

Table 1 :

Data Rate	Rate Tolerance In %
50	+/–2.5
75	+/–2.5
110	+/–2.5
150	+/–2.5
200	+/–2.5
300	+/–2.5
600	+ 1 / –2.5
1200	+ 1 / –2.5
2400	+ 1 / –2.5
3600	+ 1 / –2.5
4800	+ 1 / –2.5
7200	+ 1 / –2.5
9600	+ 1 / –2.5
12000	+ 1 / –2.5
14400	+ 1 / –2.5
19200	+ 1 / –2.5
38400	*
57600	*

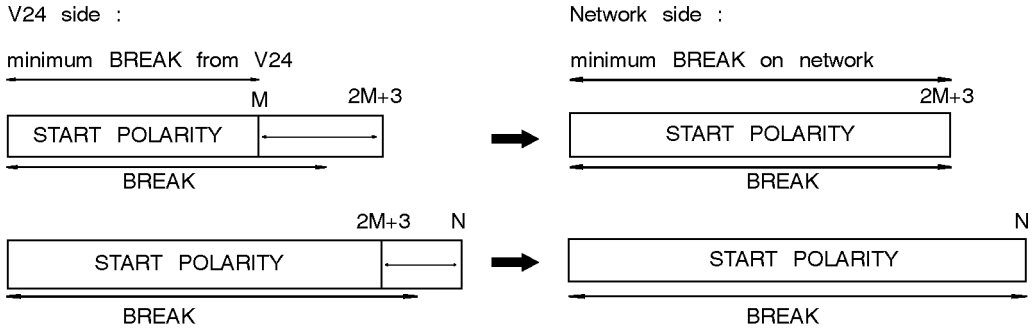
ECMA 102/V110 (except*) specification for ASYNC speeds.

Data Path

As stated earlier, local / end to end flow control and IPE re-entering modes can be implemented with the TRAC (and APPENDIX, register set : CONF and TFRM registers).

For V25bis protocol implementation the associated microprocessor is used. The TRAC connects its V24 interface to parallel µP port (UART feature). Once the call is established the UART block is connected back to RA0 for frame processing (APPENDIX, register set : CONF register).
Local and remote loopback may also be programmed (APPENDIX, register set : TFRM register)

Figure 1.



Smart Modem

When working in transparent mode (no µP action, data are going straight from V24 (103) input to DOUT output), the 29C93A may be programmed to detect an escape character and report it to the µP (via an interrupt). To do this, the user should follow several steps summarized below :

- An escape sequence is 1, 2 or 3 word length. This length is stored in ESCMOD register.
- Only the first word of the sequence (loaded in ESCVAL register) will be compared with each of the incoming V24 data.
- The detection of this word in the stream is reported in ESCSTA register (BEG bit = beginning of sequence detected = 1) if it is enabled in ESCMOD register (EIBEG bit = 1).
- When the first character of the escape sequence is detected, the remaining data (until the sequence length is reached) are stored in a FIFO (at address 0F = ESCR). These data may be removed (filtered) from the data stream or sent toward the distant terminal depending on FSEQ bit in ESCMOD register.
- When the number of data received from the beginning of the sequence is equal to the sequence length, the END status bit in ESCSTA register is set to 1 if mask bit EIEND = 1 in ESCMOD.
- In one of the BEG or END bit is set, the ESC bit = global escape status bit will be set to 1 and will involve an active level on $\overline{INT}$ pin if unmasked (AIESC bit in MASK register = 1).
- Then the TRAC will automatically configure itself to “transmit flow control” mode (that is equivalent to EPA = 1 in CONF register) if AUTO bit is set to 1 in ESCMOD register. In that case, the FC bit in ESCSTA will report the new configuration. EPA bit will remain unchanged.
- Then user can read the FIFO (via ESCR) in order to check if the received sequence is the expected one. Two pointers are available in the ESCSTA register :
  - WPT which points at the last received character (particularly useful to determine which is the last character received when the end of the sequence is not detected after a given delay).
  - RPT which points at the next character to read.
- Spurious sequence : if FSEQ = 1 (sequence remove from data stream), data may be lost if we do not pass automatically to flow control mode (we could not be able to insert this spurius sequence in the stream if characters follow).

Synchronous Block

The TRAC handles all ECMA 102 speeds for synchronous transmissions (see table 2). For speeds up to 19200 bps, a 80 bit frame is used. Above 19200 bps we will have :

For 48 kbps, a special 32 bits frame. It will handle the X, SA/SB process on the X, S1, S3, S4 bits.

For 56 kbps, a 64 bit frame without inband signalling (8th bit forced high, see & 5.5 of ECMA 102).

For 64 kbps, the TRAC will be transparent (with no frame and no inband signalling). This speed will also be used for Inband Parameters Exchange (IPE).

Interface to ISDN Driver

B Channel

The TRAC can be programmed to interface with various synchronous serial buses (and so, with most of S0 interface circuits on the market). Some of them are described in APPENDIX (register set, CLKSEL register).

The TRAC can also be programmed to transmit data on B1 or B2 channel (B2 bit in TFRM register). DOUT output will be in high impedance state except during B1 or B2. It means there will be no status/command exchange between TRAC and other ISDN circuit(s).

Transmit window width programming is made according to intermediate speed (bit V3...0 in CLKSEL register). Outside that window, DOUT will be in high impedance allowing data multiplexing according to I460. Appropriate FSK sync. pulses must be provided for each TRAC connected on the same DOUT line.

Table 2 :

Data Rate	Intermediate Rate
600	8kbps
1200	8kbps
2400	8kbps
4800	8kbps
7200*	16kbps
9600	16kbps
12000*	32kbps
14400*	32kbps
19200	32kbps
48000	SINGLE STEP ADAPTATION
56000	SINGLE STEP ADAPTATION
64000	SINGLE STEP ADAPTATION

* As stated earlier the Network Independent Clock (NIC) mode will be supported by TRAC except for 7200/14400 bps.

Network Independent Clock

For SYNC transmission using Network Independent Clock, phase difference between network and V24 clocks (R1 rate) must be measured (see &8 of ECMA 102), that is to say between :

– a 20xR1 clock network synchronized generated from a 2048, 1536, 512 or 192 kHz clock connected to NREF input using a DPLL and a 12 or 7 MHz master clock.
– and a receive bit-timing sync. clock : V24 - 113 NETWORK INDEPENDENT TRANSMIT CLOCK (ITCLK).

Microprocessor Interface and Clocks

The TRAC has a 8 bit slave µP interface including :

– 8 bit parallel data port
– 4 bit address port for internal register selection
– 1 interrupt output, each interrupt source can be selectively masked (except loss of synchroni-zation interrupt).
– 1 Chip Select input
– RD/WR control inputs

The TRAC master clock MCLK (used by the UART baud generator) must be 12.288 MHz or 7.68 MHz (selected by an internal mode register). The TRAC also has a RESET input to clear internal registers and state machines.

V24 Interchange Circuits

- All output interchange circuits can be monitored using the µP interface (via CMOD register at 00 address, fig. 3a). They also can be driven by SA, SB, and × bits recovered from incoming frame (except $\overline{\text{RING}}$ fig. 3b.). For example, in the “END TO END” flow control situation, the 105 interchange line may be driven either by $\overline{\text{CTS}}$ bit in CMOD register or by × bit from incoming frame depending on $\overline{\text{ECTS}}$ bit (also in CMOD register, figures 3a, 3b, 4b).

NOTE : X bit can only be driven by $\overline{\text{EX}}$ bit in CFRM register (fig. 4a).

- Input interchange circuits 105 ($\overline{\text{RTS}}$) and 108 ($\overline{\text{DTR}}$) are continuously sampled and stored in EMOD (0a address) register. They can drive the associated SA, SB bits in outgoing frame (fig. 5a). In the opposite case, SA and SB can be driven independently in CFRM register (fig. 5b).

NOTE : Adaptation to X21 protocol controller (such as MHS 29C921) may be achieved using 108 ($\overline{\text{DTR}}$) V24 input as C (Command) X21 circuit and 107 ($\overline{\text{DSR}}$ V24 output as I (Indicate) X21 circuit.

Inband Parameter Exchange

Because the R line does not provide the capability of OUT-OF-BAND signalling (like the D channel with the S line), the V110 (APPENDIX I, 1988) or ECMA123

recommendation define an INBAND PARAMETER EXCHANGE (IPE) protocol to support :

– the transfer of the END-TO-END information required for the compatibility checking of data calls,
– an exchange of terminal adaptor parameter information, and
– an exchange of information related to maintenance operations.

Four IPE user data/intermediate rates are also recommended :

Table 3 :

Connection Type	IPE User Rate
unrestricted 64 kb/s	64 kb/s sync
restricted 64 kb/s	56 kb/s sync
32 kb/s intermediate rate	19.2 kb/s async
16 kb/s intermediate rate	9.6 kb/s async

Recommended user data/intermediate rates

The 29C93A supports IPE for all these speeds (and even for all RA0 synchronous rates) but character filte-ring works only at 64 or 56 kb/s (with synchronous data).

Synchronous IPE also requires transmission of at least 32 times for each command byte. This feature is avail-able in the TRAC. A repeated transmission is obtained by writing in IPEBUFF register. TDI status bit will appear in INTO register after each transmission, but no interrupt is generated on INT pin, even if it is unmasked (AITD = 1 in MASK register. To stop the repetition (for example to send high-low IPE data bytes) we just have to write a byte in TDBUFF, which will be shifted only once. Then the transmitter sends “1” (INACTIVE character), and TDI bit is set until a new datum or command is written in TDBUFF or IPEBUFF.

Summary

a) synchronous IPE (synchronous primary mode)

– on DIN/DOUT : bytes aligned with FSK network clock (no start bit, no frame),
– user data rate : 56 or 64 KBPS
– for restricted 64 kb/s rate, the MSB of the byte must be set to 1.
– byte filtering in reception. (see table 4)
– byte transmission with auto-repeat capability (using IPEBUFF register).

b) asynchronous IPE (asynchronous primary mode)

– on DIN/DOUT : rate adaptation (V110/ ECMA102) ==> FRAME,
– asynchronous format (START + STOP),
– user data rate : 600 to 19200 kb/s.

Byte Filtering

Table 4 :

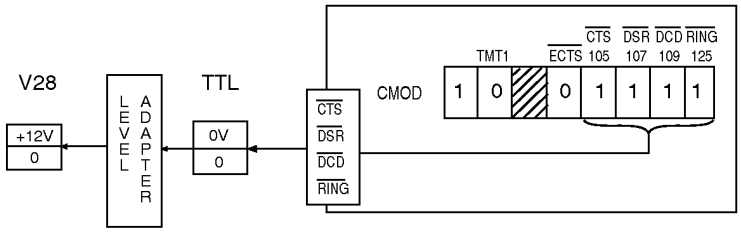
	Value (H)	Message
COMMAND	E0	PARAM-0
	E2	PARAM-4
	E4	PARAM-2
	E6	X_START
	E8	PARAM-1
	EA	RA-VERSION
	EC	PARAM-3
	EE	MAINTENANCE
STATUS	FA	READY
	FB	FILL
	FE	IDLE
	FF	INACTIVE

Power Down

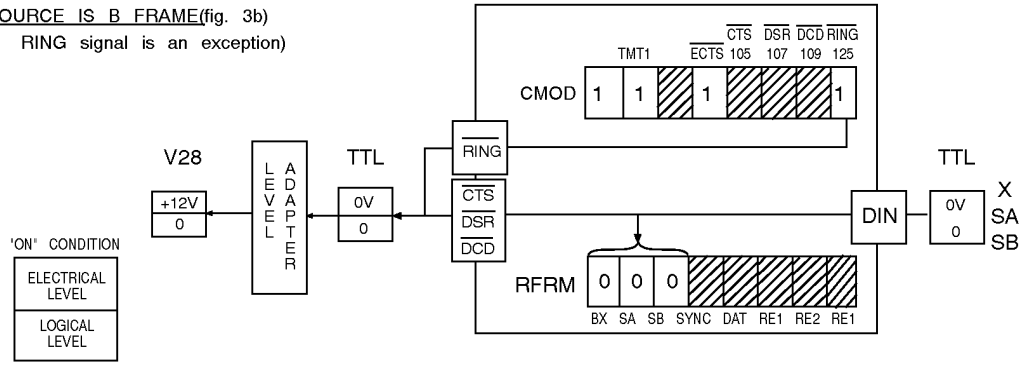
Driving pin $\overline{\text{PDWN}}$ low activates the power down mode. Once in power down, most of the signals (see table 5) are disconnected to reduce power consumption. The TRAC is thus isolated from its environment (this feature is useful for board testing).

V24 SIGNALS (from 29C93A)

a) SOURCE IS CMOD REGISTER (fig. 3a)

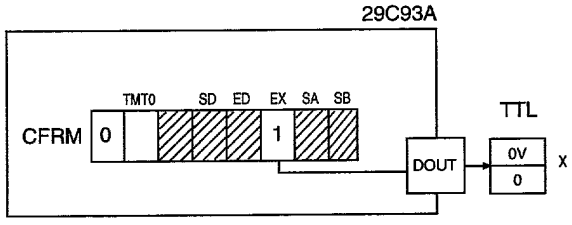


a) SOURCE IS B FRAME (fig. 3b)
(the RING signal is an exception)

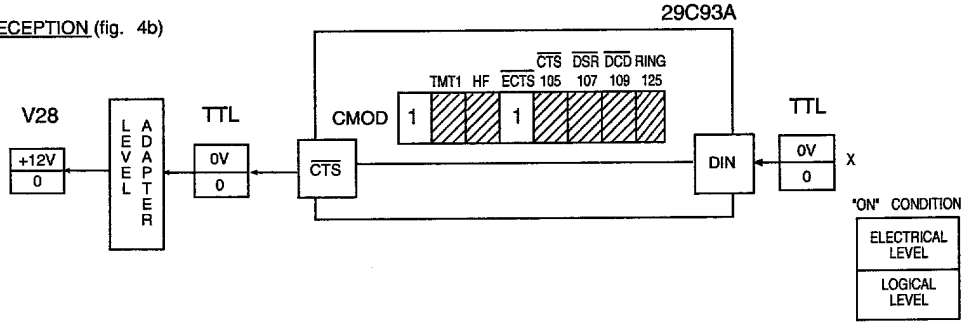


BIT MANAGEMENT

a) TRANSMISSION (fig. 4a)

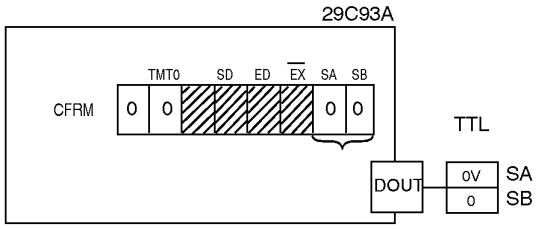


b) RECEPTION (fig. 4b)



a) SOURCE IS CFRM REGISTER (fig. 5a)

V24 SIGNALS
SA/SB GENERATION



a) SOURCE IS MODEM (fig.5b)

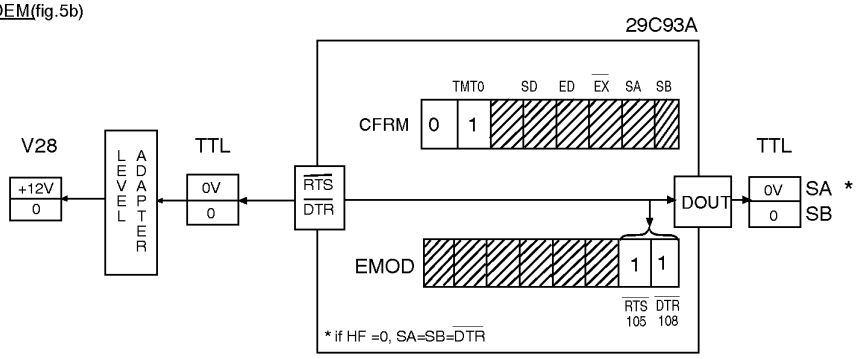


Table 5 : Power Down Mode.

Pin	Input	Output
D0:D7	DISCONNECTED	HI-Z
A0:A3	DISCONNECTED	-
CS	DISCONNECTED	-
RD	DISCONNECTED	-
WR	DISCONNECTED	-
INT	-	FORCED HIGH
BCLK	DISCONNECTED	-
MCLK	DISCONNECTED	-
NREF	DISCONNECTED	-
DIN	DISCONNECTED	-
DOUT	-	HI-Z
FSK	DISCONNECTED	-
ITCLK	DISCONNECTED	-
TCLK	-	FORCED HIGH
RCLK	-	FORCED HIGH
TXD	-	-
RXD	-	FORCED HIGH
RTS	-	-
CTS	-	FORCED HIGH
DSR	-	FORCED HIGH
DTR		-
DCD	-	FORCED HIGH
RING	-	FORCED HIGH
RESET	-	-

Appendix – Register Set

NAME	ADD	RESET								RD/WR
CMOD	00H	81H	1	TMT1	HF	$\overline{\text{ECTS}}$	$\overline{\text{CTS}}$	$\overline{\text{DSR}}$	$\overline{\text{DCD}}$	RING	R/W
CFRM	00H	00H	0	TMT0	-	SD	ED	$\overline{\text{EX}}$	SA	SB	R/W
CONF	01H	00H	AT	AS	EPA	SPA	LOCAL	APRIM	TINC	RNIC	R/W
TFRM	02H	00H	-	RFILT	SPRIM	TBL	BL	TBD	VD	B2	R/W
CLKSEL	03H	00H	BTYP1	BTYP0	REF1	REF0	V3	V2	V1	V0	R/W
ASCLK	04H	20/40H	-	TRSEL	RRSEL	AR4	AR3	AR2	AR1	AR0	R/W
FASYNC	05H	00H	H0	NS1	NS0	ND1	ND0	P2	P1	P0	R/$\overline{\text{W}}$
MASK	06H	00H	AIB	AIESC	AISX	AIPAR	AITD	AIRL	AITL	AIRD	R/W
RLBUFF	07H	0CH	LOCAL RECEIVE BUFFER								R
TLBUFF	07H	00H	LOCAL TRANSMIT BUFFER								W
RDBUFF	08H	00H	DISTANT RECEIVE BUFFER								R
TDBUFF	08H	00H	DISTANT TRANSMIT BUFFER								$\overline{\text{W}}$
RFRM	09H	EFH	BX	SA	SB	SYNC	DAT	RE3	RE2	RE1	R
ERRTD	09H	-	TRANSMISSION TO DISTANT WITH WRONG PARITY								W
EMCD	0AH	*	-	-	-	-	-	-	$\overline{\text{RTS}}$	$\overline{\text{DTR}}$	R
ERRTL	0AH	-	TRANSMISSION TO LOCAL WITH WRONG PARITY								$\overline{\text{W}}$
INT0	0BH	00H	ISEL	PARL	RLI	TLI	PARD	DSX	RDI	TDI	R
IPEBUFF	0BH	-	IPE COMMAND TRANSMIT BUFFER								W
INT1	0CH	00H	ISEL	ESC	BRKL	OVR24	-	DSYNC	BRKD	OVRS	R
ERKT	0CH	-	-	-	BRKL	-	-	-	EBKD	-	$\overline{\text{W}}$
ESCMOD	0DH	00H	0	FSEQ	AUTO	EIEND	EIBEG	ENESC	LONG1	LONG0	R/$\overline{\text{W}}$
ESCSTA	0EH	00H	ENESC	FC	RPT1	RPT0	WPT1	WPT0	END	BEG	R
ESCR	0FH	0CH	ESCAPE SEQUENCE RECEIVED (3 BYTES MAX)								R
ESCVAL	0FH	00H	PROGRAMMABLE ESCAPE VALUE								$\overline{\text{W}}$

* depends on circuit input states

CMOD ADDRESS = 00H RESET = 81H R/W MODEM SIGNAL CONTROL REGISTER

MSB LSB

1	TMT1	HF	$\overline{ECTS}$	$\overline{CTS}$	$\overline{DSR}$	$\overline{DCD}$	RING
				106	107	109	125

TMT1 : $\overline{DSR}$/$\overline{DCD}$ MODEM SIGNALS SOURCE SELECT.

TMT1 = 0 – Source is CMOD register :
$\overline{DSR}$ pin = not $\overline{DSR}$ bit,
$\overline{DCD}$ pin = not $\overline{DCD}$ bit.

TMT1 = 1 – Source is incoming frame :
$\overline{DSR}$ pin = SA = SB if HF = 0,
= SA if HF = 1,
$\overline{DCD}$ pin = SB

HF : HALF/FULL DUPLEX – X21 (active when TMT1=1)
HF = 0 – FULL DUPLEX / X21
$\overline{DSR}$ (I) pin = SA = SB.
HF = 1 – HALF DUPLEX
$\overline{DSR}$ pin = SA,
$\overline{DCD}$ pin = SB,

$\overline{ECTS}$: $\overline{CTS}$ PIN SELECT
$\overline{ECTS}$ = 0 – $\overline{CTS}$ pin = not $\overline{CTS}$ bit,
$\overline{ECTS}$ = 1 – $\overline{CTS}$ pin = × value from incoming frame.

$\overline{CTS}$: COMPLEMENTARY VALUE OF $\overline{CTS}$ (CLEAR TO SEND-106) PIN WHEN $\overline{ECTS}$ = 0

$\overline{DSR}$: COMPLEMENTARY VALUE OF $\overline{DSR}$ (DATA SET READY-107) PIN WHEN TMT1 = 0
TMT1 = 0 – $\overline{DSR}$ pin = not $\overline{DSR}$ bit.

$\overline{DCD}$: COMPLEMENTARY VALUE OF $\overline{DCD}$ (DATA CARRIER DETECT-109) PIN
WHEN TMT1 = 0
TMT1 = 0 – $\overline{DCD}$ pin = not $\overline{DCD}$ bit.

RING : COMPLEMENTARY VALUE OF RING (CALLING INDICATOR-125) PIN
RING pin = not RING bit

NOTE : READ OPERATION
CMOD register is read at address 0 if the MSB of the recovered byte is set to 1 (otherwise, CFRM register is concerned). For 2 successive read operations at address 0, we always will recover 2 different values of this MSB, that means that one time CMOD register will be read (MSB=1), the other time CFRM register will be read (MSB=0).

READ operation at 0	:	n	n+ 1	n+2.....
MSB recovered	:	1	0	1.....
REGISTER concerned	:	CMOD	CFRM	CMOD .....

CFRM ADDRESS = 00H RESET = 00H W FRAME SIGNAL CONTROL REGISTER

MSB LSB

0	TMT0	.	SD	ED	$\overline{EX}$	SA	SB

TMT0 : SA/SB/D FRAME BIT SELECT.
TMT0 = 0 – Source is CFRM register :
SA (bit frame) = SA (bit register)
SB (bit frame) = SB (bit register)
TMT0 = 1 – Source is MODEM :
SA (bit frame) = $\overline{DTR}$ pin
SB (bit frame) = $\overline{DTR}$ pin if HF = 0
= $\overline{RTS}$ pin if HF = 1

SD : DATA BIT SELECT
SD = 0 – D = ED (for example ED = 0 during resync mode)
SD = 1 – D = TxD (103)

ED : DATA BIT TO BE TRANSMITTED WHEN SD = 0

$\overline{EX}$: COMPLEMENTARY VALUE OF X BIT TO BE TRANSMITTED

SA : VALUE OF SA BIT TO BE TRANSMITTED WHEN TMT0 = 0

SB : VALUE OF SB BIT TO BE TRANSMITTED WHEN TMT0 = 0

NOTE : READ OPERATION (SEE CMOD REGISTER)

CONF ADDRESS = 01H RESET = 00H R/W CONFIGURATION REGISTER

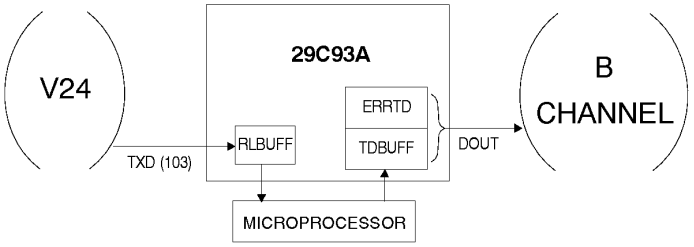
MSB LSB

AT	AS	EPA	SPA	LOCAL	APRIM	TNIC	RNIC

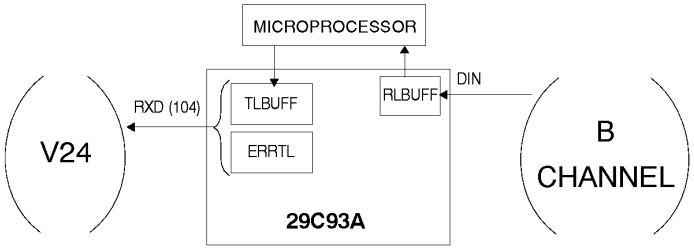
AT : FRAME ENABLE
Frame transmit and synchronization enable after communication has been established.
AT = 0 – DOUT pin high impedance,
AT = 1 – transmit enable.

AS : ASYNC / SYNC SELECT
AS = 0 – Synchronous,
AS = 1 – Asynchronous.

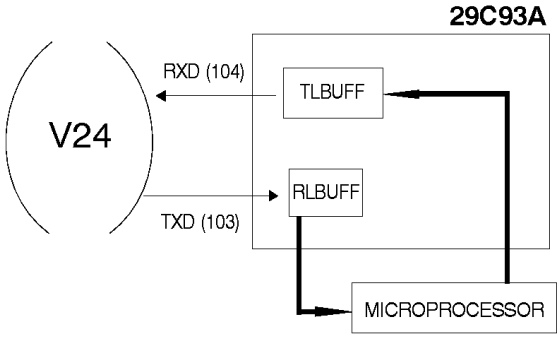
EPA : TRANSMIT FLOW CONTROL
TDBUFF/RLBUFF register access through µP bus allowing local flow control between TRAC and near end terminal.
EPA = 0 – access locked,
EPA = 1 – access enabled :



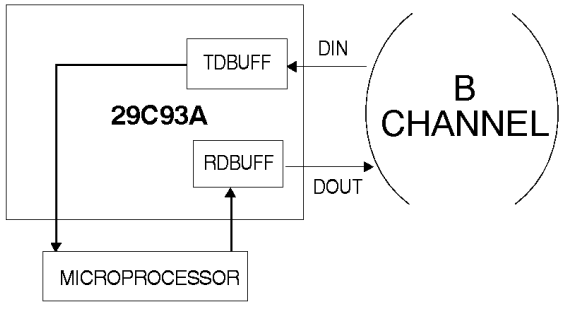
SPA : RECEIVE FLOW CONTROL
TLBUFF/RDBUFF register access through µP bus allowing distant flow control operation between TRAC and far-end terminal.
SPA=0 – access locked,
SPA=1 – parallel input/output enabled :



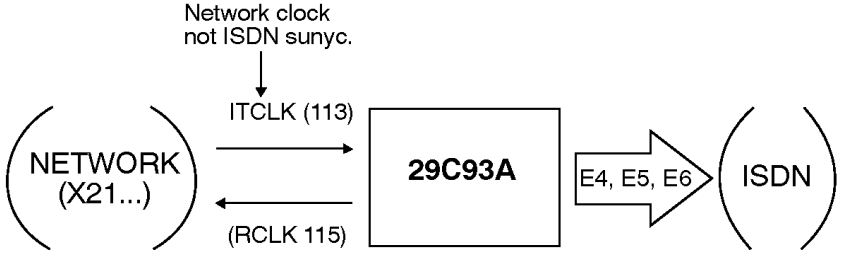
LOCAL : LOCAL MODE ENABLE (for V25bis)
TLBUFF/RLBUFF registers access through µP bus allowing exchange with local terminal.
LOCAL = 0 – access locked,
LOCAL = 1 – parallel input/output enabled.



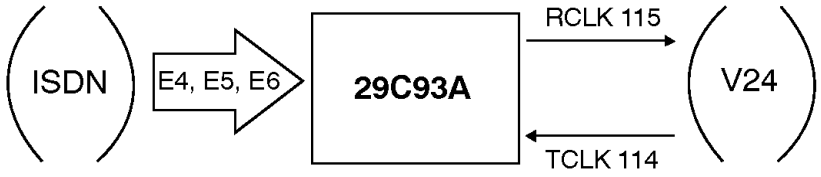
APRIM : ASYNCHRONOUS PRIMARY MODE ENABLE (for IPE re-entering)
RDBUFF/TDBUFF registers access through µP bus allowing exchange with B channel.
APRIM = 0 – access locked,
APRIM = 1 – access enabled :



TNIC : ALLOWS E4, E5, E6 GENERATION IN TRANSMIT FRAME (except for 7.2/12/14.4 kbps, comparison between ITCLK (113) and ISDN network clocks).
TNIC = 0 – no compensation,
TNIC = 1 – compensation enabled – E bit generation.



RNIC : E4, E5, E6 bit decoding – TCLK/RCLK clock compensation.
RNIC = 0 – no compensation,
RNIC = 1 – compensation enabled – E bit decoding.



TFRM ADDRESS = 02H RESET = 00H R/W TRANSMIT FRAME REGISTER

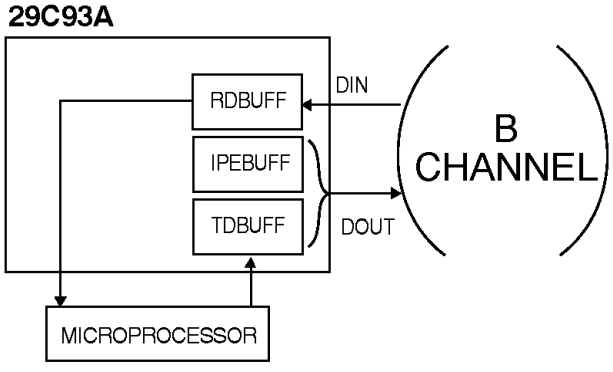
MSB LSB

.	RFILT	SPRIM	TBL	BL	TBD	BD	B2

RFILT : FILTERING FOR INCOMING DATA

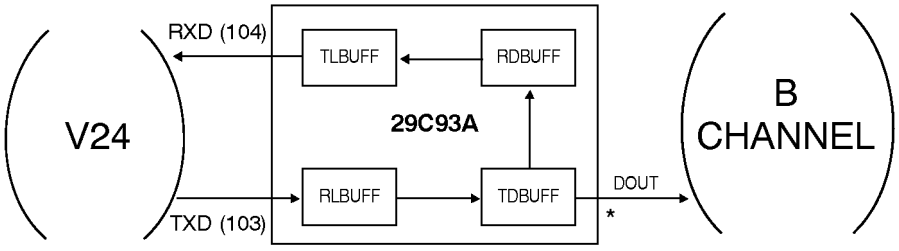
SPRIM : SYNCHRONOUS PRIMARY ACCESS (FOR INBAND PARAMETER EXCHANGE – 56/64 kbps)
Enables parameter exchange after communication is established and before synchronization

RFILT	SPRIM	
0	0	no primary access
0	1	access to 64 (or 56) kbps synchronous primary mode
1	0	reserved
1	1	access to 64 (or 56) kbps synchronous primary mode with IPE facilities (command byte transmission with auto repeat via IPEBUFF and command byte filtering in reception)



TBL : DATA OUTPUT ENABLE (with LOCAL LOOPBACK mode only)
TBL = 0 – data not enabled on B output (forced to 1)
TBL = 1 – data enabled on B output during local loopback

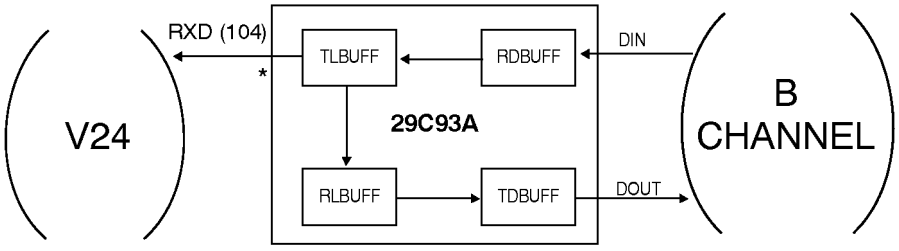
BL : LOCAL LOOPBACK
B transmitter output connected to B receiver input
BL = 0 – no loopback
BL = 1 – loopback enabled



* Enabled by TBL bit

TBD : DATA OUTPUT ENABLE (with DISTANT LOOPBACK mode only)
TBD = 0 – data not enabled on 104 output (forced to 1)
TBD = 1 – data enabled on 104 output during distant loopback

BD : DISTANT LOOPBACK
TxD (103) connected to RxD (104)
BD = 0 – no loopback
BD = 1 – loopback enabled



* Enabled by $\overline{TBD}$ bit

B2 : B1/B2 CHANNEL SELECT
B2 = 1 – B2 select
B2 = 0 – B1 select

CLKSEL ADDRESS = 03H RESET = 00H R/W CLOCK SELECTION REGISTER

MSB LSB

BTYP1	BTYP0	REF1	REF0	V3	V2	V1	V0

BTYP1	BTYP0	IN	OUT	BCLK	PPG
0	0	↑	↓	1	no
0	1	↓	↑	1	no
1	0	↓	↑	1/2	no
1	1	↓	↑	1	YES

REF1	REF0	NREF (kHz)
0	0	2048
0	1	1536
1	0	512
1	1	192

IN = input sampling edge OUT = output driving edge

PPG = no – input/output on B channel side are simultaneous and synchronized with FSK frame sync clock.
PPG = yes – master/slave mode, input/output operations occur alternatively within 1/8 kHz period.
DOUT is used as I/O pin.

EXAMPLES :

BTYP 1	BTYP 0	BCLK (kHz)*	FSK	
0	0	192		B1 B2 B3
0	1	128		B1 B2
1	0	512		B1 B2 M C/I
				IN OUT
1	1	512		B1 B2 M C/I B1 B2 M C/I

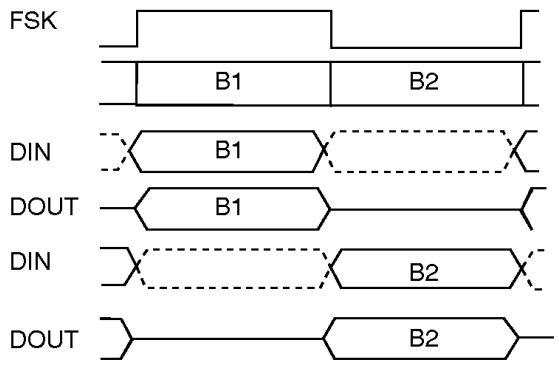
* minimum BCLK values to have the channels as indicated.

V3..0 : SYNCHRONOUS TE RATE SELECT, ASYNC TE INTERMEDIATE RATE SELECT

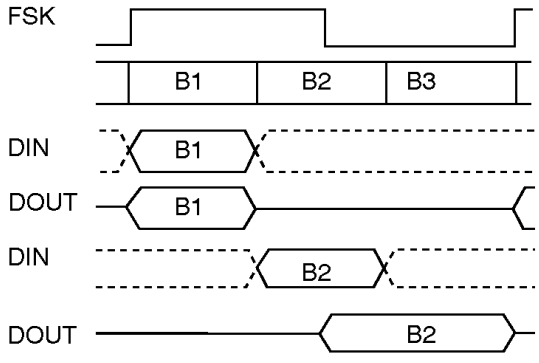
V3	V2	V1	V0	Terminal Speed	Intermediate Speed	Frame	Repetition Coef.
0	0	0	0	64000 bps	64 kHz	TRANSP.	1
0	0	0	1	600 bps	8 kHz	80	8
0	0	1	0	1200 bps	8 kHz	80	4
0	0	1	1	2400 bps	8 kHz	80	2
0	1	0	0	3600 bps**	8 kHz	80	1
0	1	0	1	4800 bps	8 kHz	80	1
0	1	1	0	7200 bps*	16 kHz	80	1
0	1	1	1	9600 bps	16 kHz	80	1
1	0	0	0	12000 bps*	32 kHz	80	1
1	0	0	1	14400 bps*	32 kHz	80	1
1	0	1	0	19200 bps	32 kHz	80	1
1	0	1	1	38400 bps**	64 kHz	32	1
1	1	0	0	48000 bps	64 kHz	32	1
1	1	0	1	56000 bps	64 kHz	64	1
1	1	1	0	57600 bps**	64 kHz	TRANSP.	1
1	1	1	1	64000 bps	64 kHz	TRANSP.	1

* For 7200/12000/14400 bauds Network Independent Clock is not supported even when programmed. "–" reserved.
** Values not defined in ECMA 102/V110 recommendations.

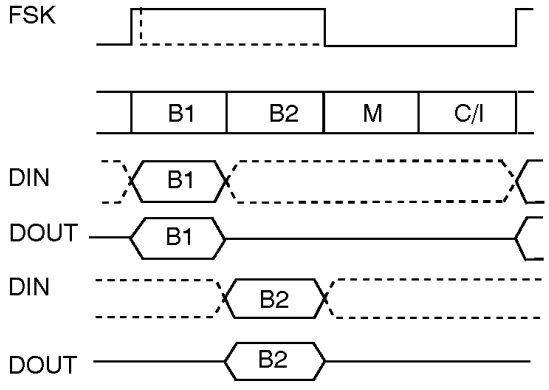
a) SSI OPERATING MODE



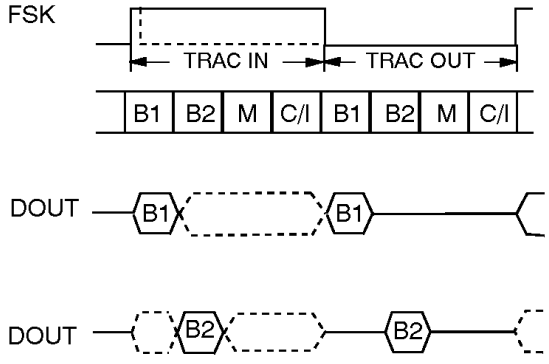
b) AMD OPERATING MODE



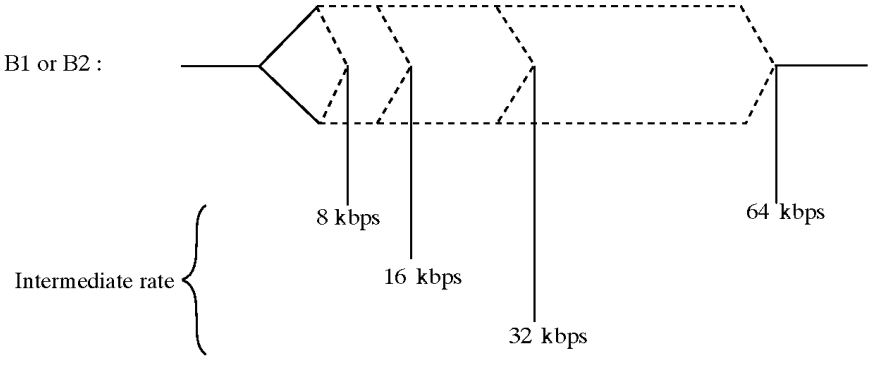
c) IOM OPERATING MODE



d) SLD OPERATING MODE



CHANNEL DETAIL (to allow I460 multiplexing)



ASCLK ADDRESS = 04H RESET = 40H/20H R/W ASYNCHRONOUS CLOCK PROGRAMMING REGISTER

MSB LSB

.	TRSEL	RRSEL	AR4	AR3	AR2	AR1	AR0

TRSEL	RRSEL	
0	0	NOT USED
0	1	Receive (remote to local) asynchronous rate select
1	0	Transmit (local to remote) asynchronous rate select
1	1	Same asynchronous rate on receive and transmit side.

For write operation, if receive and transmit rates are different, the user should do two operations, one for each side. If both are the same, a single write is sufficient.

For read operation, TRSEL and RRSEL bits show which side (s) is (are) concerned.

AR4..AR0 Asynchronous rate selection

AR4	AR3	AR2	AR1	AR0	ASYNC. RATE
0	0	0	0	0	50 bps
0	0	0	0	1	75 bps
0	0	0	1	0	110 bps
0	0	0	1	1	150 bps
0	0	1	0	0	200 bps
0	0	1	0	1	300 bps
0	0	1	1	0	600 bps
0	0	1	1	1	1200 bps
0	1	0	0	0	2400 bps
0	1	0	0	1	3600 bps
0	1	0	1	0	4800 bps
0	1	0	1	1	7200 bps
0	1	1	0	0	9600 bps
0	1	1	0	1	12000 bps
0	1	1	1	0	14400 bps
0	1	1	1	1	19200 bps
1	0	0	0	0	38400 bps
1	0	0	0	1	57600 bps

FASYNC ADDRESS = 05H RESET = 00H R/W ASYNCHRONOUS FORMAT REGISTER

MSB LSB

H0	NS1	NS0	ND1	ND0	P2	P1	P0

H0 : MCLK SELECT (BAUD RATE GENERATOR)

0 7.68 MHz clock select

1 12.288 MHz clock select

NS1..0 : STOP BIT NUMBER SELECT (ASYNC)

NS1	NS0	NUMBER OF STOP BITS
0	0	1 parity bit plus 1 stop bit
0	1	1 stop bit
1	0	1.5 stop bit
1	1	2 stop bits

ND1..0 : BIT NUMBER PER CHARACTER (ASYNC)

ND1	ND0	BITS/CHARACTER
0	0	UNUSED
0	1	5 BITS
1	0	7 BITS
1	1	8 BITS

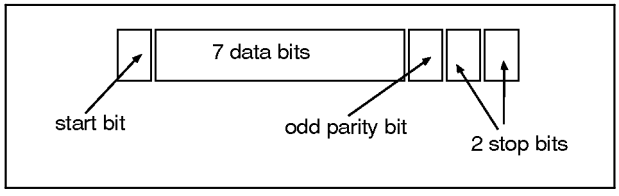
P2..0 : ASYNC PARITY ADAPTATION TO TERMINAL PARITY

P2	P1	P0	
0	0	0	NO PARITY
0	0	1	odd
0	1	0	even
1	0	0	forced to 0
1	1	1	forced to 1

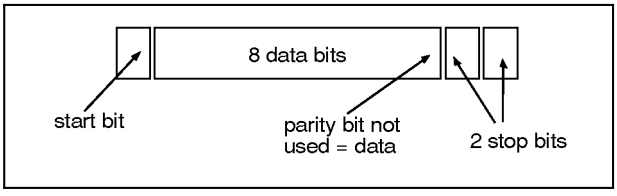
NOTES :
a) when [NS1, NS0] is different than [0, 0], the format given by [ND1, ND0] is parity included. If no parity is used, the parity bit is taken as a normal data bit.

EXAMPLES :

FASYNC = x1111001 / PARITY ODD



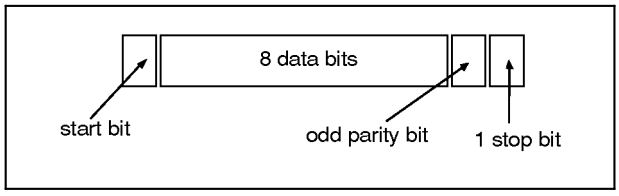
FASYNC = x1111000 / NO PARITY



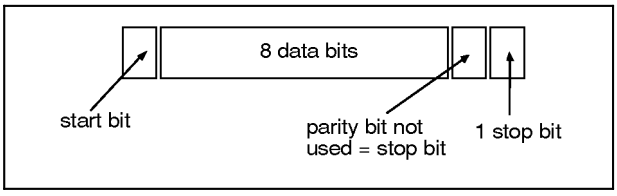
b) When [NS1, NS0] is equal to [0, 0], the format given by [ND1, ND0] is with parity not included. The parity bit and one stop bit are added after 5 or 8 bits.

EXAMPLES :

FASYNC = x0011001 / PARITY ODD



FASYNC = x0011000 / NO PARITY



MASK ADDRESS = 06H RESET = 00H R/W INTERRUPT ENABLE REGISTER

MSB LSB

AIB	AIESC	AISX	AIPAR	AITD	AIRL	AITL	AIRD

ALL LEVELS ACTIVE HIGH

AIB : BREAK DETECTION ENABLE
AIESC : ESCAPE CHARACTER DETECTION ENABLE
AISX : RECEIVED SA/SB/X BIT CHANGE
AIRPAR : PARITY ERROR CHECK ENABLE
AITL : DATA REQUEST (TLBUF EMPTY)
AIRD : DATA READY (RDBUFF FULL)

RLBUFF ADDRESS = 07H RESET = 00H R RECEIVE LOCAL REGISTER (V24 to µP)

MSB							LSB
LOCAL SIDE RECEIVED DATA							

TLBUFF ADDRESS = 07H RESET = 00H W TRANSMIT LOCAL REGISTER (µP to V24)

MSB							LSB
LOCAL SIDE TRANSMITTED DATA							

RDBUFF ADDRESS = 08H RESET = 00H R RECEIVED DISTANT REGISTER (B channel to µP)

MSB							LSB
FAR END SIDE RECEIVED DATA							

TDBUFF ADDRESS = 08H RESET = 00H W TRANSMIT DISTANT REGISTER (µP to B channel)

MSB							LSB
FAR END SIDE TRANSMITTED DATA							

RFRM ADDRESS = 09H RESET = EFH R RECEIVE FRAME STATE REGISTER

MSB							LSB
BX	SA	SB	SYNC	DAT	RE3	RE2	RE1

BX : RECEIVED X BIT STATE

SA : RECEIVED SA BIT STATE
80 BIT FRAME – S1, S3, S6, S8 STATE
32 BIT FRAME – S1, S3 STATE

SB : RECEIVED SB BIT STATE
80 bit frame – S4, S9 state
32 bit frame – S4 state

BX, SA, SB are significant only in case of sync/intermediate speeds < 48 kbps (80 bit or 32 bit frames).

SYNC : SYNCHRO STATE (RECEIVE)
This bit indicates TRAC sync state compared to received frame
SYNC = 0 – not sync
SYNC = 1 – synchronized

DAT : RECEIVED D BIT
80 BIT FRAME – D1 to D48 data bit states in received frame
64 BIT FRAME – D1 to D56 data bit states in received frame
32 BIT FRAME – D1 to D24 data bit states in received frame

RE3..1 : RECEIVED E3..1 BIT (BIT REPETITION IDENTIFICATION)

RE3	RE2	RE1	8 kbps	16 kbps	32 kbps	REP Factor
0	0	1	600			8
0	1	0	1200			4
0	1	1	2400			2
1	0	0			12000	1
1	0	1		7200	14400	1
1	1	0	4800	9600	19200	1

ERRTD ADDRESS = 09H RESET = – W TRANSMIT TO DISTANT WITH WRONG PARITY

MSB LSB

DISTANT SIDE TRANSMITTED DATA (with wrong parity)

Data written in ERRTD are transmitted toward the distant terminal with a wrong parity bit.

EMOD ADDRESS = 0AH RESET = – R MODEM SIGNALS STATE REGISTER

MSB LSB

–	–	–	–	–	–	$\overline{\text{RTS}}$	$\overline{\text{DTR}}$

$\overline{\text{RTS}}$: 105 circuit status (REQUEST TO SEND)
$\overline{\text{DTR}}$: 108 circuit status (DATA TERMINAL READY)

ERRTL ADDRESS = 0AH RESET = – W TRANSMIT TO LOCAL WITH WRONG PARITY

MSB LSB

LOCAL SIDE TRANSMITTED DATA (with wrong parity)

Data written in ERRTL are transmitted toward the distant terminal with a wrong parity bit.

INTO ADDRESS = 0BH RESET = 00H R INTERRUPT REGISTER

MSB LSB

ISEL	PARL	RLI	TLI	PARD	DSX	RDI	TDI

ISEL : INTERRUPT REGISTER SOURCE
ISEL = 0 – no status change has ocured in INT1 register.
ISEL = 1 – IA status change has occured in INT1 register.

PARL : PARITY BIT (on local side)
PARL = 1 – indicates a parity bit error has been detected in RLBUFF, reading RLBUFF resets PARL to 0.

RLI : RECEIVE LOCAL BUFFER FULL
RLI = 1 – indicates that RLBUFF is full, reading RLBUFF clears RLI.

TLI : TRANSMIT LOCAL BUFFER EMPTY
TLI = 1 – indicates that TLBUFF is empty, writting in TLBUFF clears TLI.

PARD : PARITY BIT (on distant side)
PARD = 1 – indicates a parity bit error has been detected in RDBUFF, reading RDBUFF resets PARD to 0.

DSX : FRAME SIGNALLING DATA CHANGE
DSX = 1 – indicates SA/SB/X bit status change in received frame, reading RFRM clears DSX.

RDI : RECEIVE DISTANT BUFFER FULL
RDI = 1 – indicates RDBUFF is full, reading RDBUFF clears RDI.

TDI : Transmit distant buffer empty
TDI = 1 – indicates TDBUFF is empty, writing in TDBUFF clears TDI.

IPEBUFF ADDRESS = 0BH RESET = – W IPE BUFFER

MSB LSB

IPE BUFFER

This buffer only works with 64 kbps (restricted or unrestricted) Inband Parameter Exchange mode (SPRIM bit set to 1 in TFRM register). Writing in IPEBUFF issues an auto-repeat transmission toward B channel (IPE data command should be transmitted at least 32 times).

INT1 ADDRESS = 0CH RESET = 00H R INTERRUPT REGISTER

MSB LSB

ISEL	ESC	BRKL	OVR24	–	DSYNC	BRKD	OVRS

ISEL : INTERRUPT REGISTER SOURCE
ISEL = 0 – no status change in INT1 register since last read (INT1 = 0)
ISEL = 1 – at least one status change has occured in INT1 register.

ESC : GLOBAL ESCAPE STATUS
ESC = 1 – one (or both) of the BEG and END bit is (are) active in ESCMOD register. Reading ESCMOD clears ESC.

BRKL : LOCAL BREAK RECEPTION
BRKL = 1 – indicates near end (LOCAL) BREAK detection.
Interrupt generation if AIB = 1 (MASK register).

OVR24 : V24 OVERFLOW
OVR24 = 1 – indicates V24 overrun. Indicates an attempt has been made to overwrite RLBUFF. RLBUFF keeps the last not-read value. Following data bytes coming from V24 side will be lost. Reading RLBUFF clears OVR24. Interrupt generation if AIRL = 1 (MASK register).

DSYNC : SYNC STATE CHANGE
DSYNC = 1 – indicates a synchronization status change.
An interrupt will always be generate (cannot be masked).

BRKD : DISTANT BREAK RECEPTION
BRKD = 1 – indicates far end (DISTANT) BREAK detection.
Interrupt generation if AIB = 1 (MASK register).

OVRS : B CHANNEL OVERFLOW
OVRS = 1 – indicates system overrun. Indicates an attempt has been made to overwrite RDBUFF. RDBUFF keeps the last not-read value. Following data bytes coming from B channel will be lost. Reading RDBUFF clears OVRS. Interrupt generation if AIRD = 1 (MASK register).

BRKT ADDRESS = 0CH RESET = – W BREAK TRANSMISSION

MSB LSB

–	–	EBKL	–	–	–	EBKD	–

EBKL : BREAK TRANSMISSION TO LOCAL
EBKL = 1 – involves a minimum BREAK transmission (2M+3) toward the LOCAL side.
EBKL = 0 – nothing

EBKD : break transmission to distant
EBKD = 1 – involves a minimum BREAK transmission (2M+3) toward the DISTANT side.
EBKD = 0 – nothing

ESCMOD ADDRESS = 0DH RESET = 00H R/W ESCAPE MODE REGISTER

MSB LSB

0	FSEQ	AUTO	EIEND	EIBEG	ENESC	LONG1	LONG0

FSEQ : ESCAPE SEQUENCE FILTERING
FSEQ = 0 – no filtering
FSEQ = 1 – if ENESC = 1, the data of the escape sequence (received on V24 side) are not transmitted toward B channel.

AUTO : TRANSMIT FLOW CONTROL MODE AUTOMATIC PROGRAMMING AFTER ESCAPE SEQUENCE DETECTION
AUTO = 0 – no automatic programming
AUTO = 1 – automatic mode programming after detection of the end of an escape sequence. The mode changes to TRANSMIT FLOW CONTROL mode (CMOD register remains unchanged, but the FC bit in escape status register (ESCSTA) will report the change).

EIEND : INTERRUPT ON “END OF ESCAPE SEQUENCE” ENABLE
EIEND = 0 – interrupt disabled
EIEND = 1 – interrupt on END OF ESCAPE SEQUENCE enabled

EIBEG : INTERRUPT ON “BEGINNING OF ESCAPE SEQUENCE” ENABLE
EIBEG = 0 – interrupt disabled
EIBEG = 1 – interrupt on “beginning of escape sequence” enabled

ENESC : ESCAPE SEQUENCE DETECTION ENABLE
ENESC = 0 – escape sequence detection disabled. Remainder ESCMOD register bits are inoperative
ENESC = 1 – escape sequence detection enabled. All the V24 incoming data are compared with the byte in ESCVAL register. 29C93A behaviour depends now on ESCMOD programming.

LONG1..0 : ESCAPE SEQUENCE LENGTH

LONG1	LONG0	
0	0	ESCR fifo not used. If ENSC = 1, an escape character may be detected and involve an interrupt.
0	1	The escape sequence is 1 character long. The received escape character is available in ESCR. BEG and END status bit will be active at the same time.
1	0	The escape sequence is 2 character long. 2 bytes will be available in ESCR fifo : the first which is equal to ESCVAL and the second that was following it in the stream. BEG will be set to 1 after the first reception, END after the second.
1	1	The escape sequence is 3 character long. 3 bytes will be avai lable in ESCR fifo. BEG and END status bits will be active after the 1st and the 3rd reception respectively.

ESCSTA ADDRESS = 0EH RESET = 00H R ESCAPE STATUS REGISTER

MSB LSB

ENESC	FC	RPT1	RPT0	WPT1	WPT0	END	BEG

ENESC : Copy of ENESC bit in ESCMOD register.

FC : TRANSMIT FLOW CONTROL MODE ACTIVE

FC = 0 – no mode change.

FC = 1 – TRAC enters in transmit flow control mode after the detection of an escape sequence.

RPT1..0 : READ POINTER ON ESCR FIFO

RPT1	RPT0	
0	0	
0	1	no character received (length of sequence = 0.
1	0	shows next data of the escape sequence to be read
1	1	(must be compared with WRTP1)

WPT1..0 : WRITE POINTER ON ESCR FIFO

WPT1	WPT0	
0	0	
0	1	the FIFO is empty (length of sequence = 0).
1	0	shows the number of data received from the
1	1	beginning of the escape sequence

END : END OF ESCAPE SEQUENCE

END = 0 – the number of data received since the beginning of the escape sequence is less than the length programmed.

END = 1 – the last data of the escape sequence has been received (that means, the number of data received since the beginning of the sequence is equal to the length programmed)

BEG : BEGINNING OF AN ESCAPE SEQUENCE

BEG = 0 – no escape character received.

BEG = 1 – an escape character (matching with ESCVAL register) has been detected on V24-103 line.

NOTE : all these bits will have to be ignored if ENESC = 0 (escape sequence detection disabled)

ESCR ADDRESS = 0FH RESET = 00H R ESCAPE SEQUENCE RECEIVED

MSB LSB

3 BYTE LONG FIFO

The character (s) (1, 2, 3 depending on length programmed in ESCMOD register) following an escape character detection (and including it) are written in this FIFO.

ESCVAL ADDRESS = 0FH RESET = 00H W ESCAPE CODE REGISTER

MSB LSB

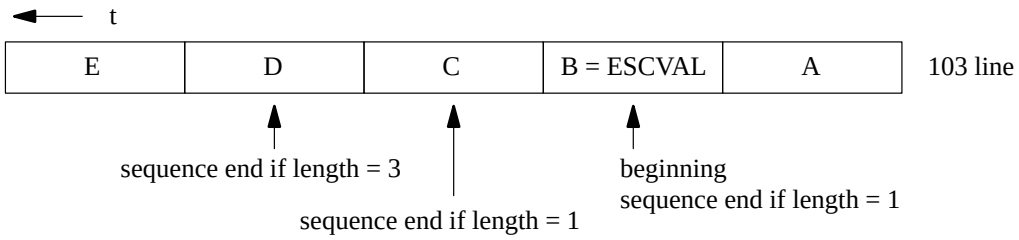
ESCAPE CODE VALUE

This register is used to detect the beginning of an “ESCAPE SEQUENCE”. If enabled by ENESC bit, all the characters received on V24-103 line will be compared with it.

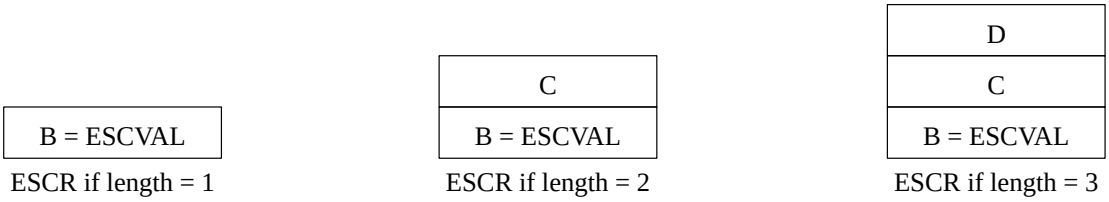
More Details About Escape Sequence

a) An escape sequence begins with an escape character (character B below) that match with ESCVAL value,

b) An escape sequence is 1 (B only), 2 (B and C) or 3 (B, C and D) character long.



c) Data included in the escape sequence are stored in ESCR fifo as they come from V24 line.



d) The escape sequence may be removed from incoming data stream (filtering)

On 103 input line side :

.....	E	end	.	begin.	A	.....

On B channel side :

.....	E	A	.....

e) Interrupts may be generated if enabled (status bit unmasked)

sequence length	first character reception	second character reception	third character reception
0	BEG	-	-
1	BEG + END	-	-
2	BEG	END	-
3	BEG	-	END

"–" no interrupt or uncompatible with sequence length.

Electrical Characteristics

Absolute Maximum Ratings

VCC to GND : . . . . . –0.3 V to + 7 V
Input/Output voltage : . . . . . –0.3 V to VCC + 0.3 V

DC Characteristics

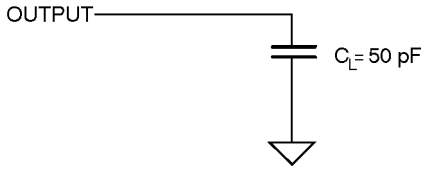
V_{CC} = 5 V ± 10 % TA = 0°C to 70°C

Parameter	Min.	Max.	Unit	Conditions
Low level input voltage VIL		1.5	V	
High level output voltage VIH	2		V	
Low level output voltage VOL		0.4	V	IOL = 13.3 mA
High level output voltage VOH	2.4		V	IOH = 13.3 mA
Input leakage current IIL/IIH	-4	+4	µA	Vin = 0 / Vin = VCCmax
3 state output leakage current IOZ	-4	+4	µA	V_{CC} = 5.5 V
Standby current ICCO		100	µA	Vin = V_{CC} or GND Outputs unloaded, CLK = GND or VCC
Operating current ICC1		20	mA	V_{CC} = 5.5 V, MCLK = 12.288 MHz VIL = GND, VIH = VCC
Operating current in Power Down mode		2	mA	V_{CC} = 5.5 V, MCLK = 12.288 MHz VIL = GND, VIH = VCC

AC Characteristics

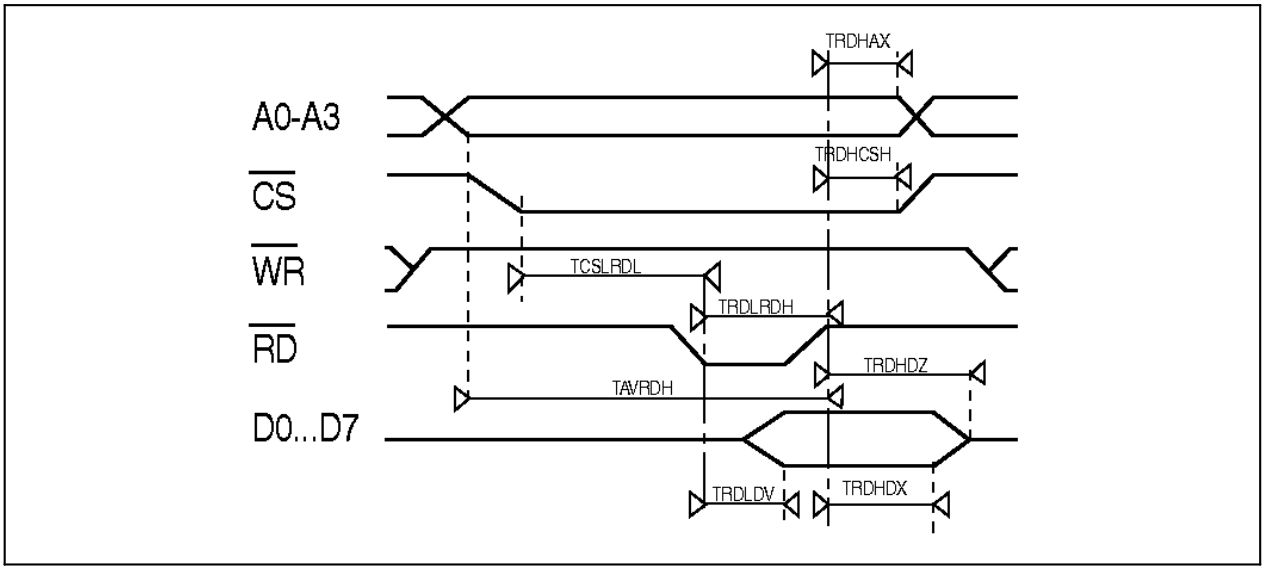
VCC = 5 V ± 10 % TA = 0 °C to 70 °C

Load Circuit



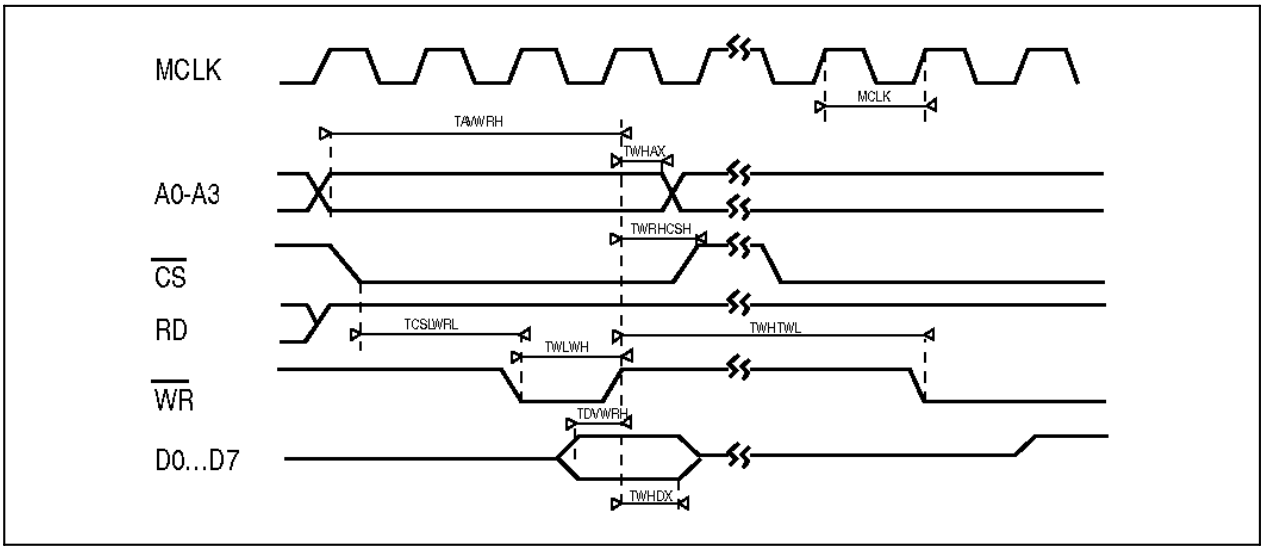
Timings

Read Cycle



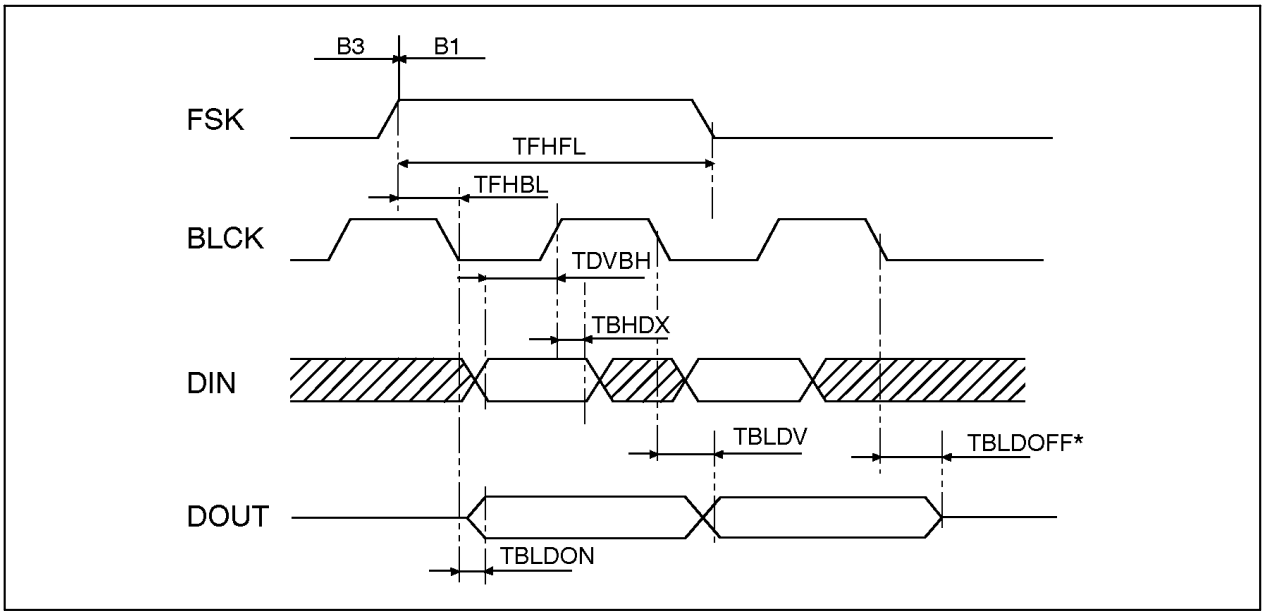
Symbol	Parameter	Min	Max	Unit
TVARDH	address valid to read high set up time	30		ns
TRDLRDH	minimum read pulse	40		ns
TCSLRDL	chip select low to read low	0		ns
TRDLDV	read low to data valid		40	ns
TRDHAX	hold address from read high	0		ns
TRDHCSH	chip select high to read high	0		ns
TRDHDX	data hold from read high	8		ns
TRDHDZ	data high Z from read high		30	ns

Write Cycle



Symbol	Parameter	Min	Max	Unit
TWLWH	minimum write pulse	20		ns
TDVWRH	data set up to write high	10		ns
TWHDX	hold data from write high	10		ns
TCSLWRL	chip select low to write low	0		ns
TWHAX	hold address from write high	10		ns
TWRHCSH	chip select high from write high	0		ns
TAVWRH	address set up to write high	12		ns
TWHTWL	write high to write low	2		MCLK

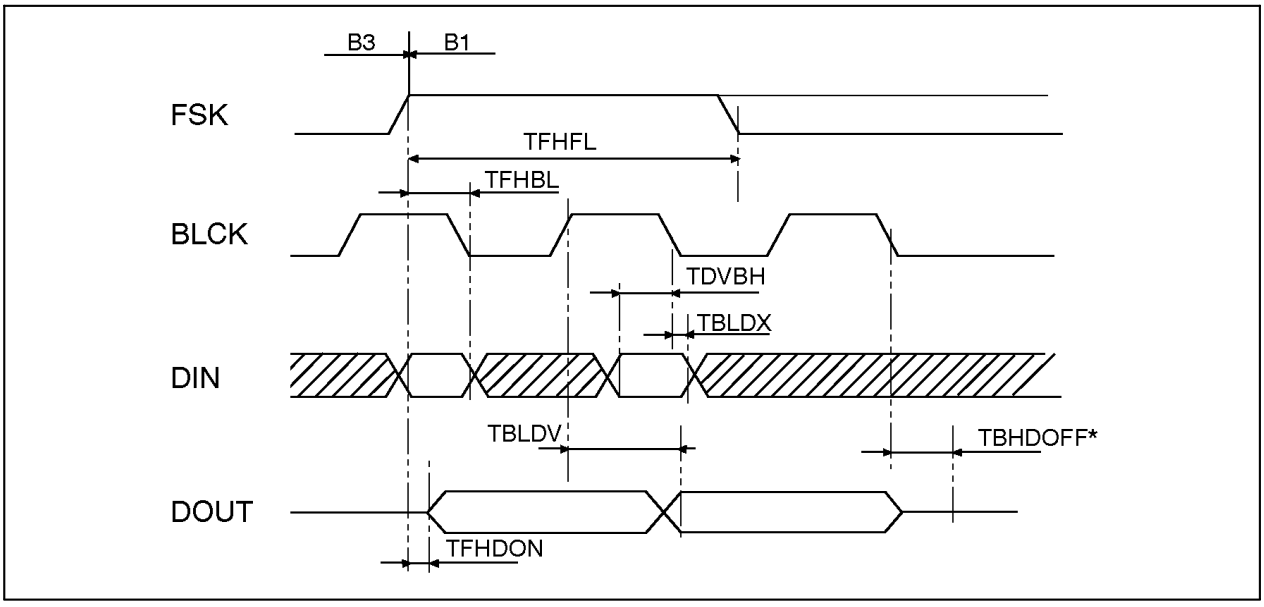
AMD Timing



* For the last data bit in the channel, here with a 16 kHz intermediate rate.

Symbol	Parameter	Min	Max	Unit
TFHBL	FSK high to BCLK low	20		ns
TFHFL	minimum FSK pulse	1		BCLK
TDVBL	data in set up to BCLK low	50		ns
TBHDX	hold data in from BCLK low	50		ns
TBLDON	data out valid from BCLK low (first data bit)		50	ns
TBLDV	data out valid from BCLK low		40	ns
TBLDOFF	data out high-Z from BCLK low (last data bit/channel)		50	ns

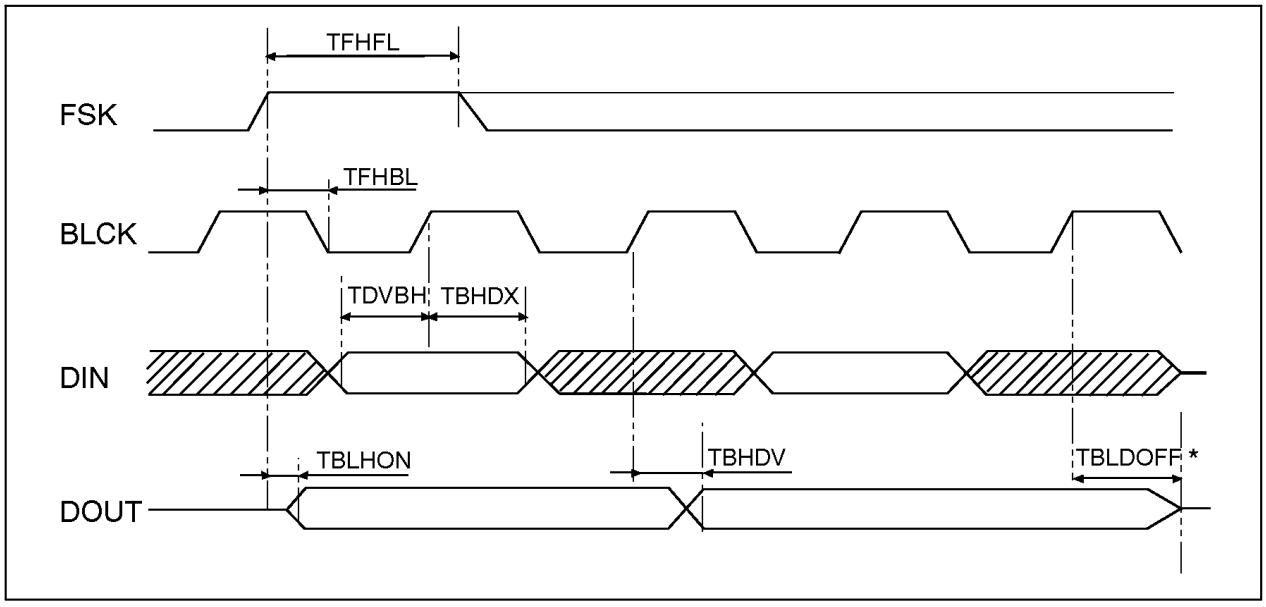
SSI Timing



* For the last data bit in the channel, here with a 16 kHz intermediate rate.

Symbol	Parameter	Min	Max	Unit
TFHBL	FSK high to BCLK low	20		ns
TFHFL	minimum FSK pulse	1		BCLK
TDVBL	data in set up to BCLK low	50		ns
TBLDX	hold data in from BCLK low	50		ns
TFHDON	data out valid from FSK high (first data bit)		50	ns
TBHDV	data out valid from BCLK high		40	ns
TBHDOFF	data out high-Z from BCLK high (last data bit/channel)		50	ns

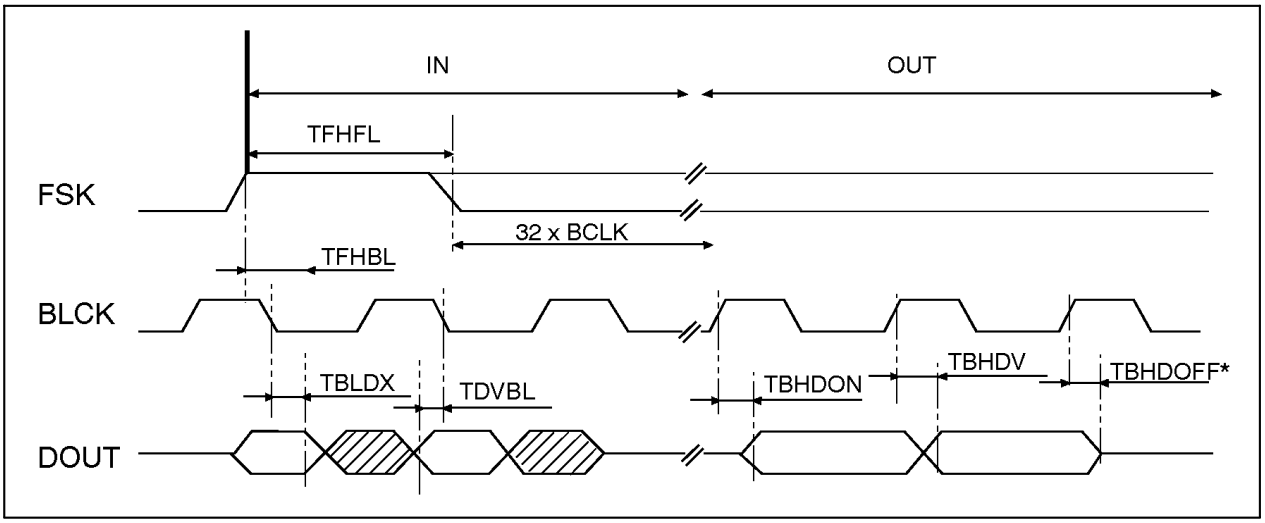
IOM Timing



* For the last data bit in the channel, here with a 16 kHz intermediate rate.

Symbol	Parameter	Min	Max	Unit
TFHBL	FSK high to BCLK low	20		ns
TFHFL	minimum FSK pulse	1		BCLK
TDVBL	data in set up to BCLK high	50		ns
TBHDX	hold data in from BCLK high	50		ns
TFHDON	data out valid from FSK high (first data bit)		50	ns
TBHDV	data out valid from BCLK high		40	ns
TBHDOFF	data out high-Z from BCLK high (last data bit/channel)		50	ns

SLD Timing



* For the last data bit in the channel, here with a 16 kHz intermediate rate.

Symbol	Parameter	Min	Max	Unit
TFHBL	FSK high to BCLK low	20		ns
TFHFL	minimum FSK pulse	1		BCLK
TDVBL	data in set up to BCLK low	50		ns
TBLDX	hold data in from BCLK low	50		ns
TBHDON	data out valid from BCLK high (first data bit)		50	ns
TBHDV	data out valid from BCLK high		40	ns
TBHDOFF	data out high-Z from BCLK high (last data bit/channel)		50	ns

Ordering Information

Ø	F	29C93A
TEMPERATURE RANGE Ø COMMERCIAL 0 TO 70 ˚C I INDUSTRIAL −40 TO 85 ˚C	PACKAGE : F = PQFP	Part number 29C93A